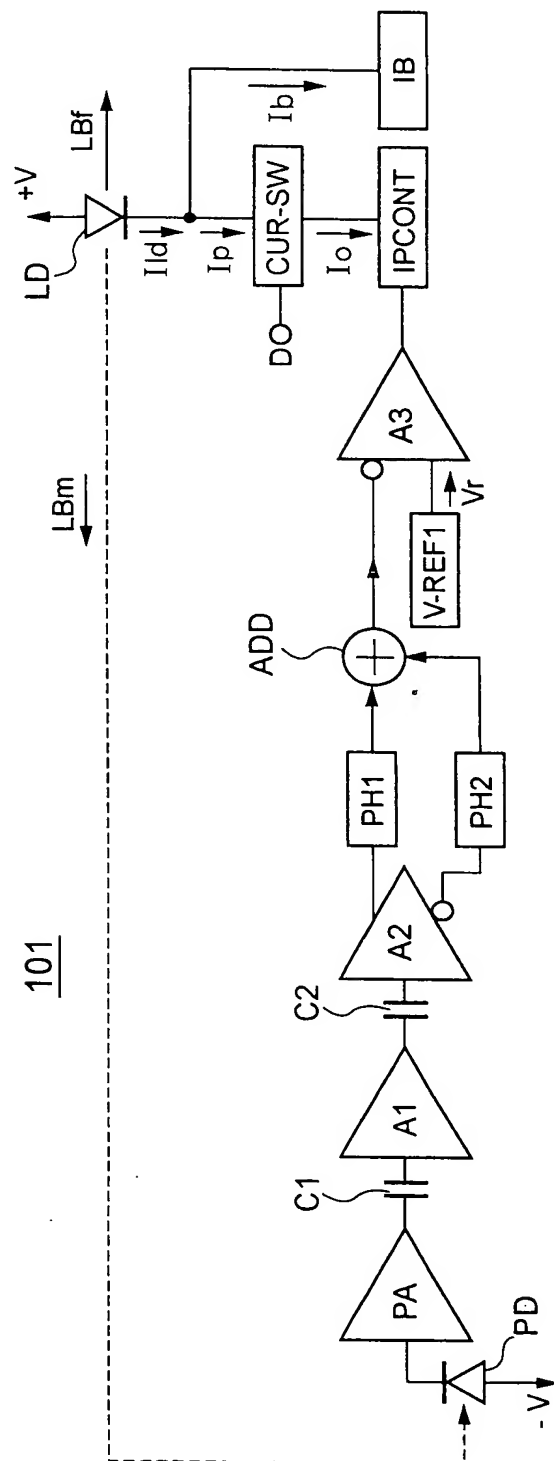


FIG. 2



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FIG. 3

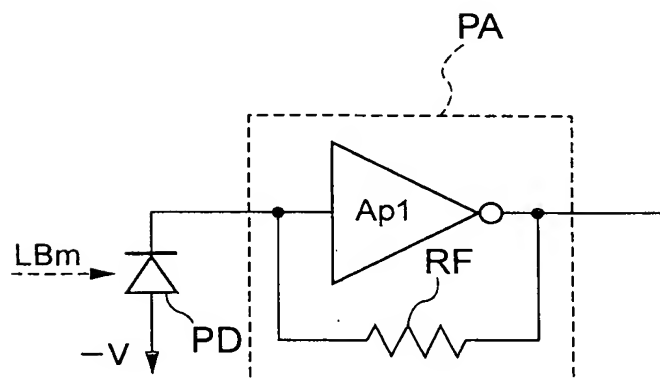


FIG. 4

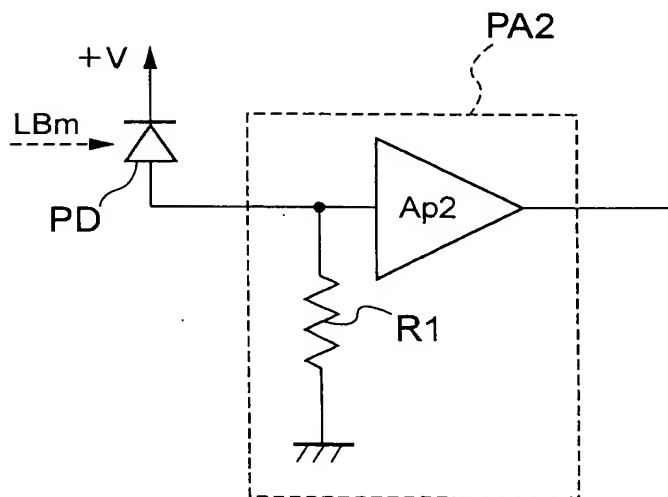


FIG. 5A

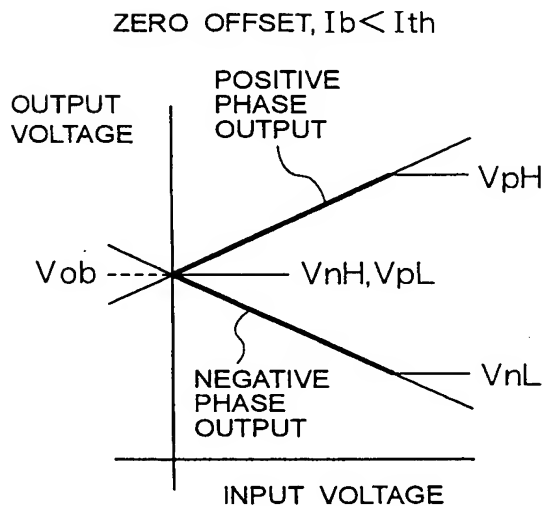


FIG. 5B

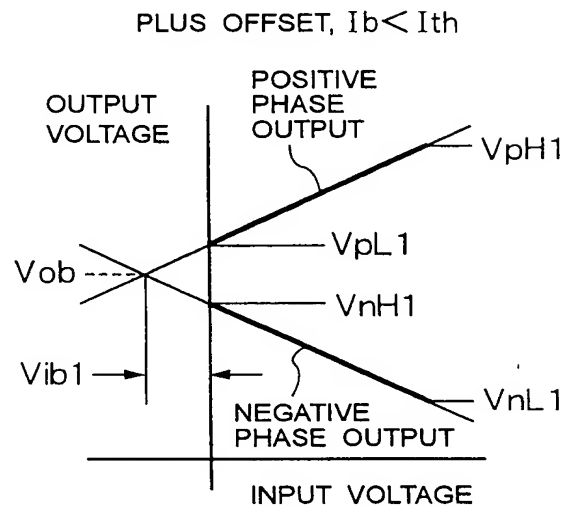


FIG. 5C

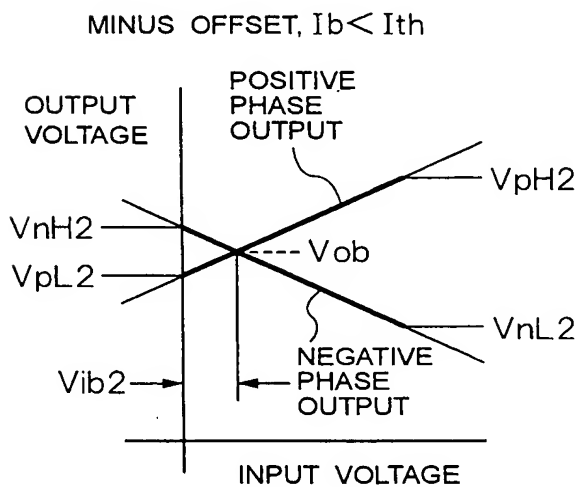
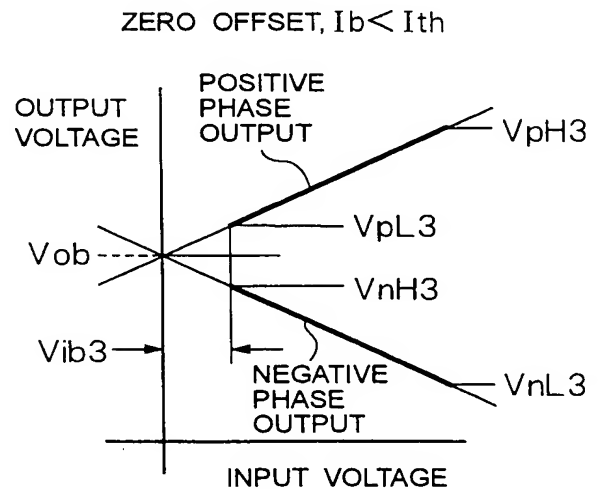
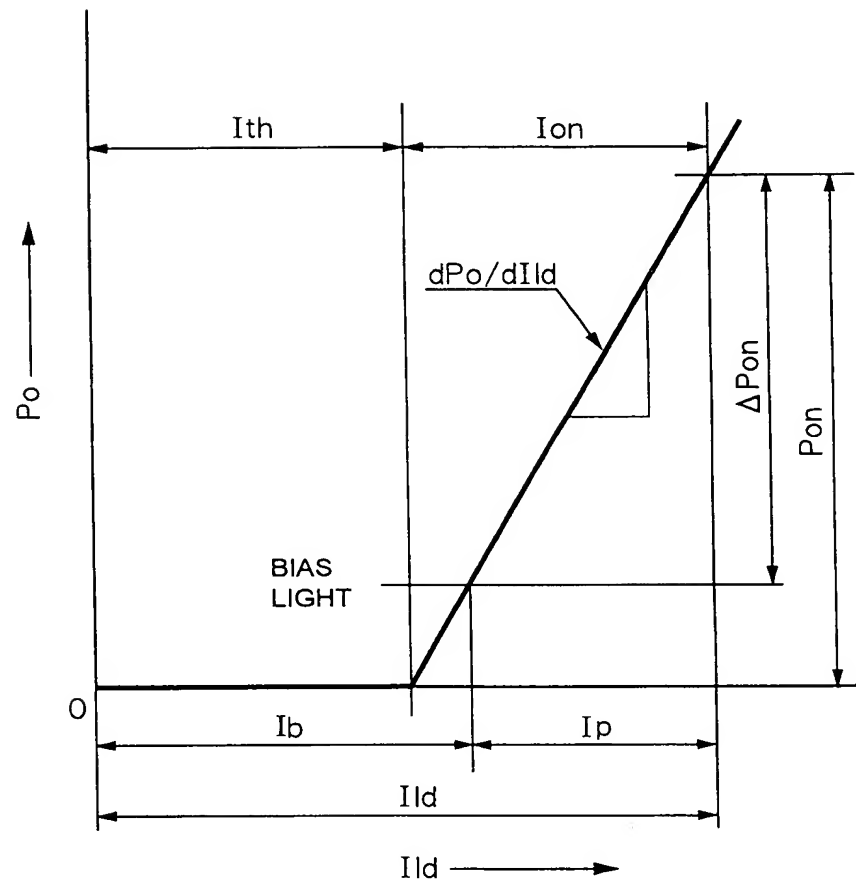


FIG. 5D



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FIG. 6



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FIG. 7A

ZERO OFFSET
 SAME "1/0" RATIO
 AC COUPLED INPUT

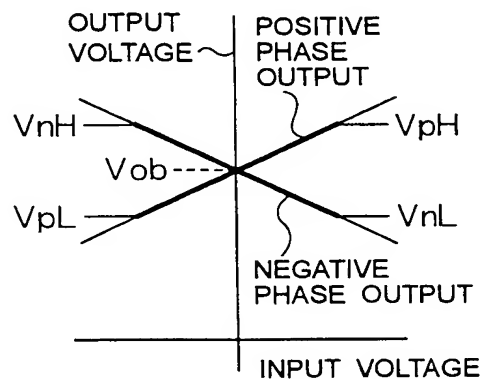


FIG. 7B

ZERO OFFSET
 AC COUPLED INPUT

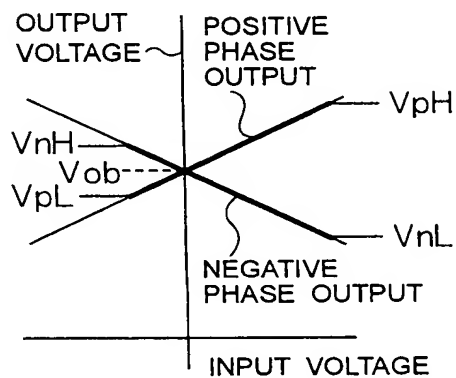


FIG. 7C

ZERO OFFSET
 AC COUPLED INPUT

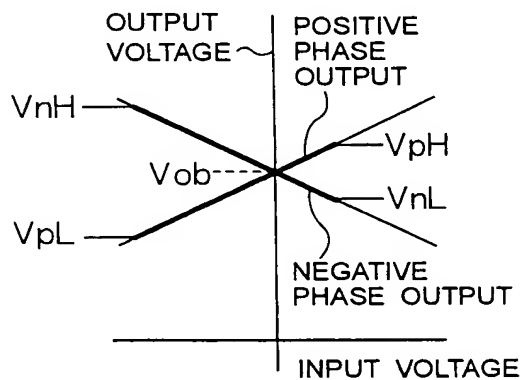
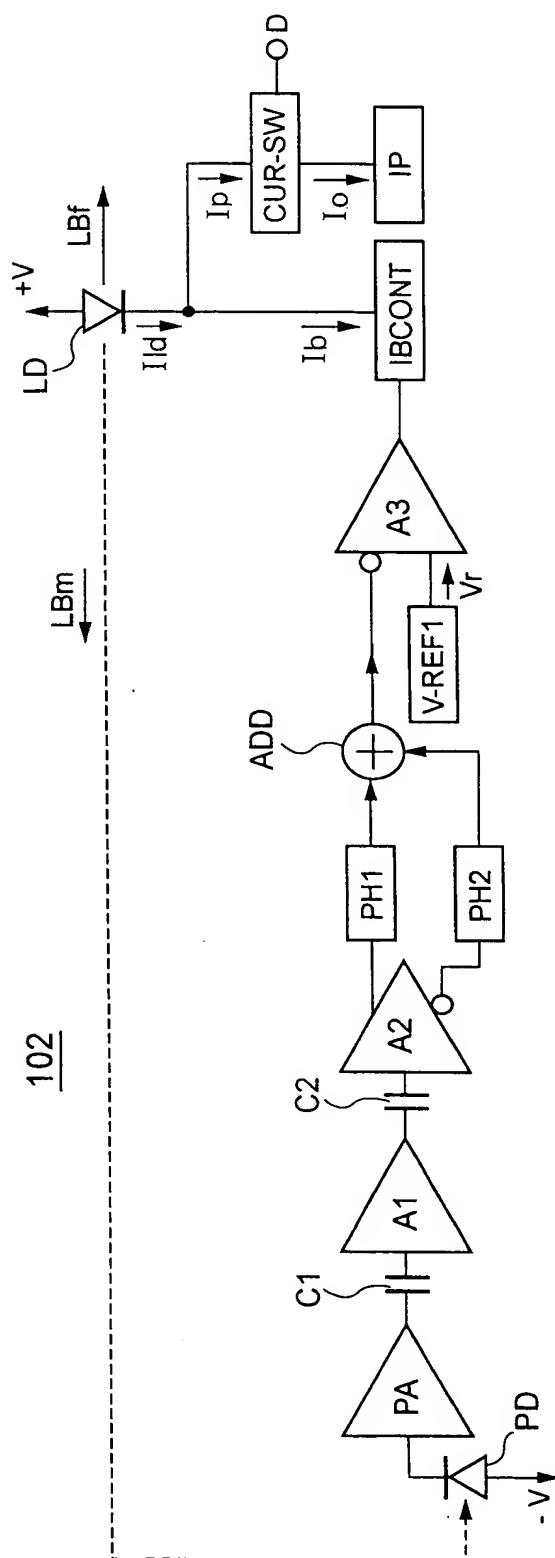


FIG. 8



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FIG. 9

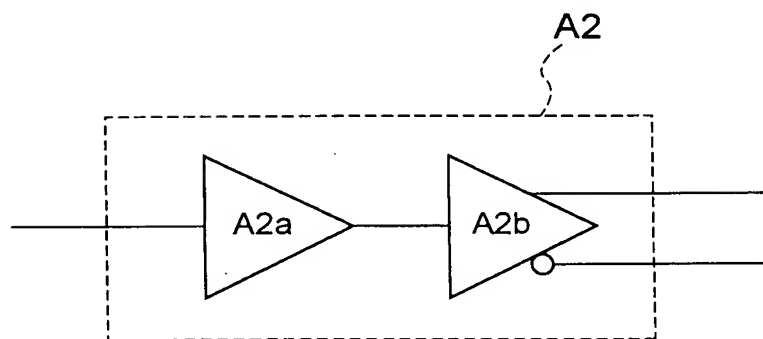


FIG. 10

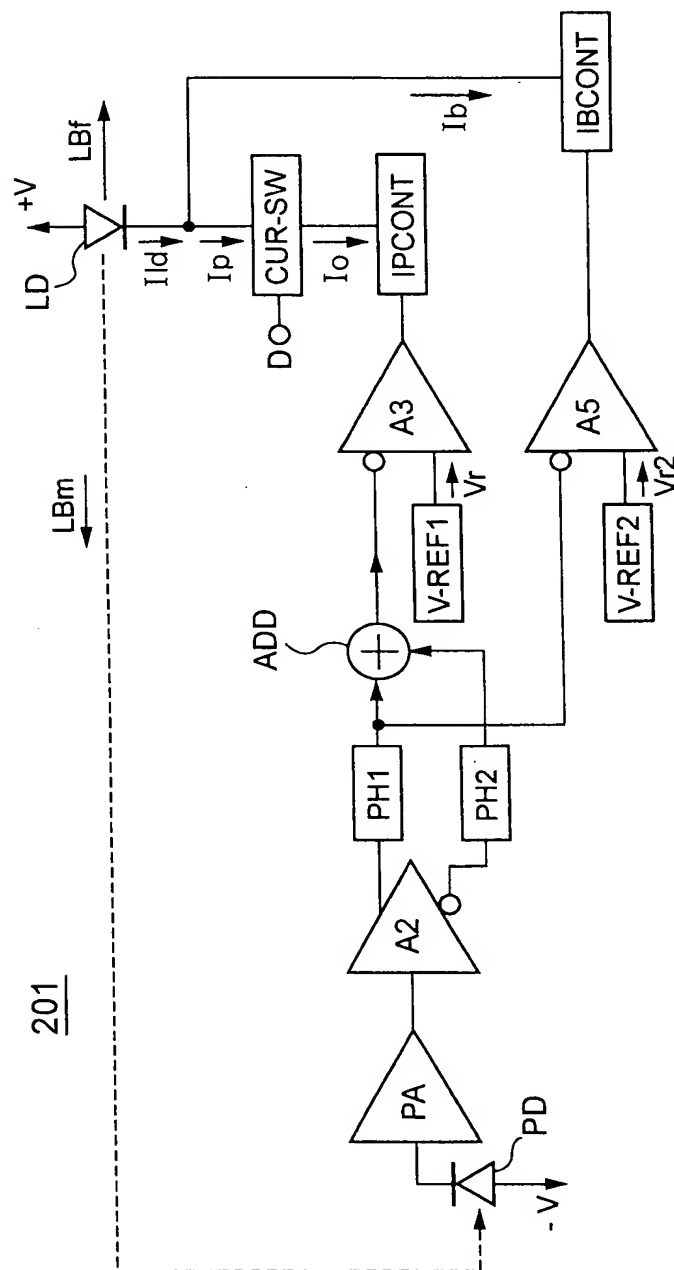
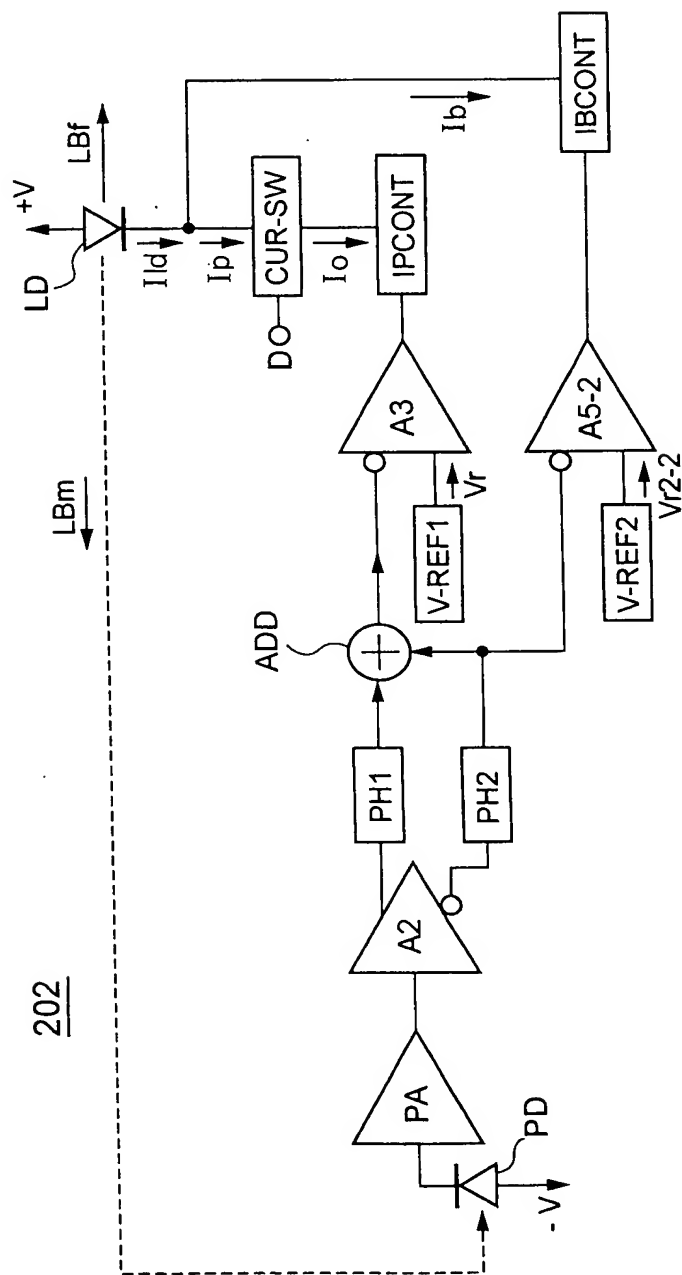


FIG. 11



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FIG. 12A

ZERO OFFSET
 $I_b \doteq I_{th} (I_b > I_{th})$

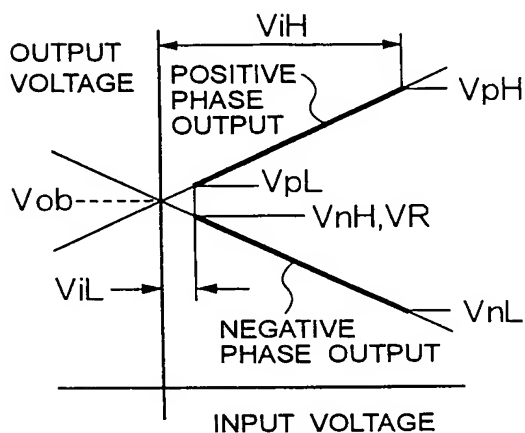


FIG. 12B

MINUS OFFSET
 $I_b > I_{th}$

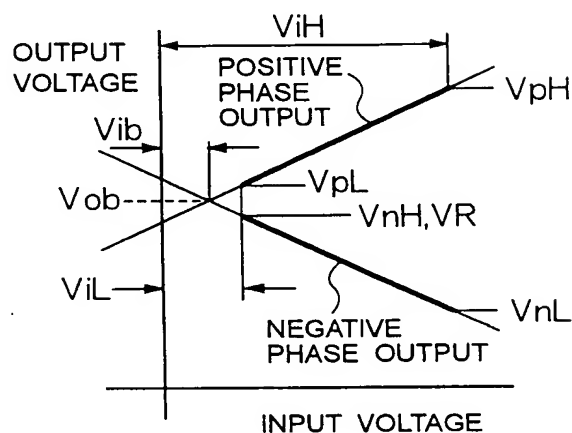


FIG. 12C

PLUS OFFSET
 $I_b > I_{th}$ (LOW VR CASE)

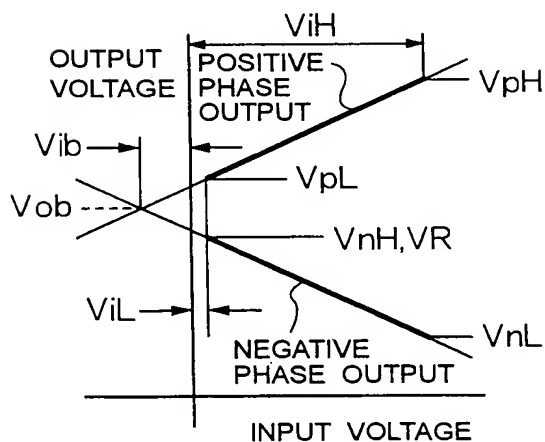


FIG. 12D

PLUS OFFSET
 $I_b = 0$ (HIGH VR CASE)

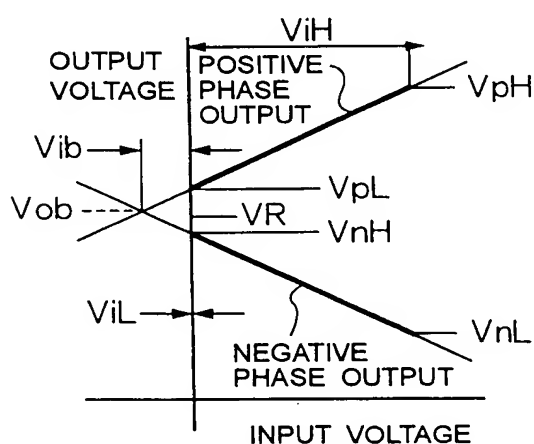


FIG. 13

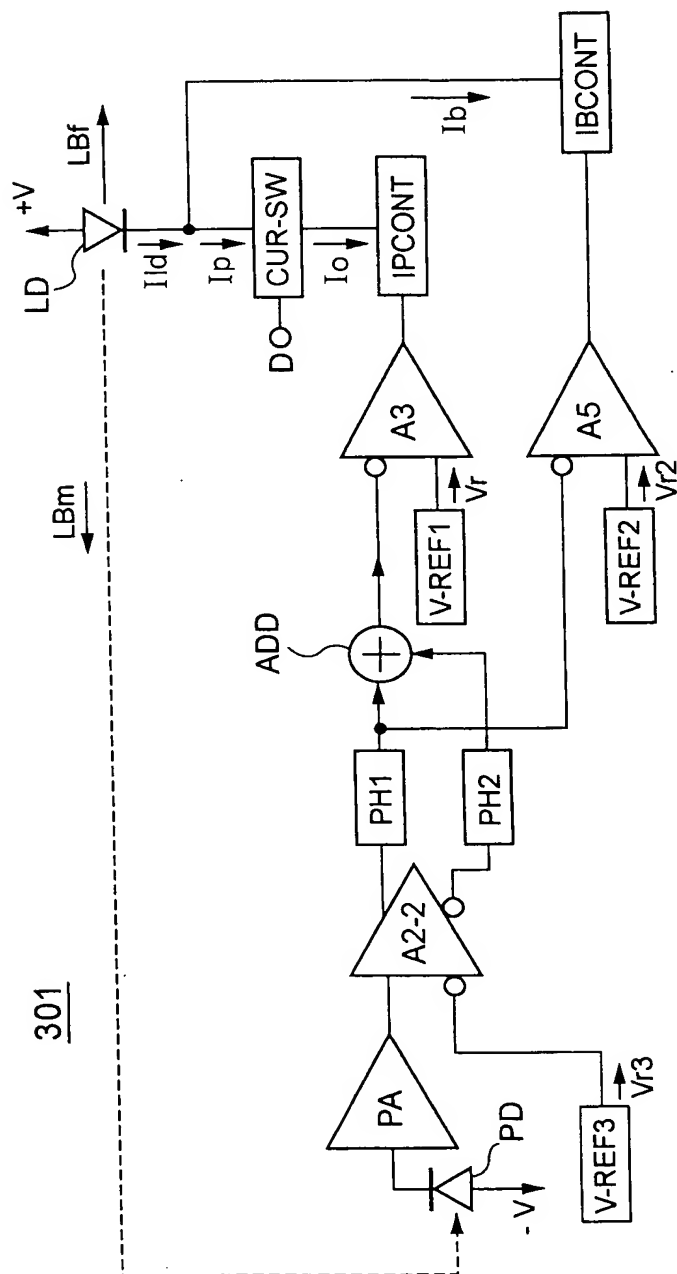


FIG. 14

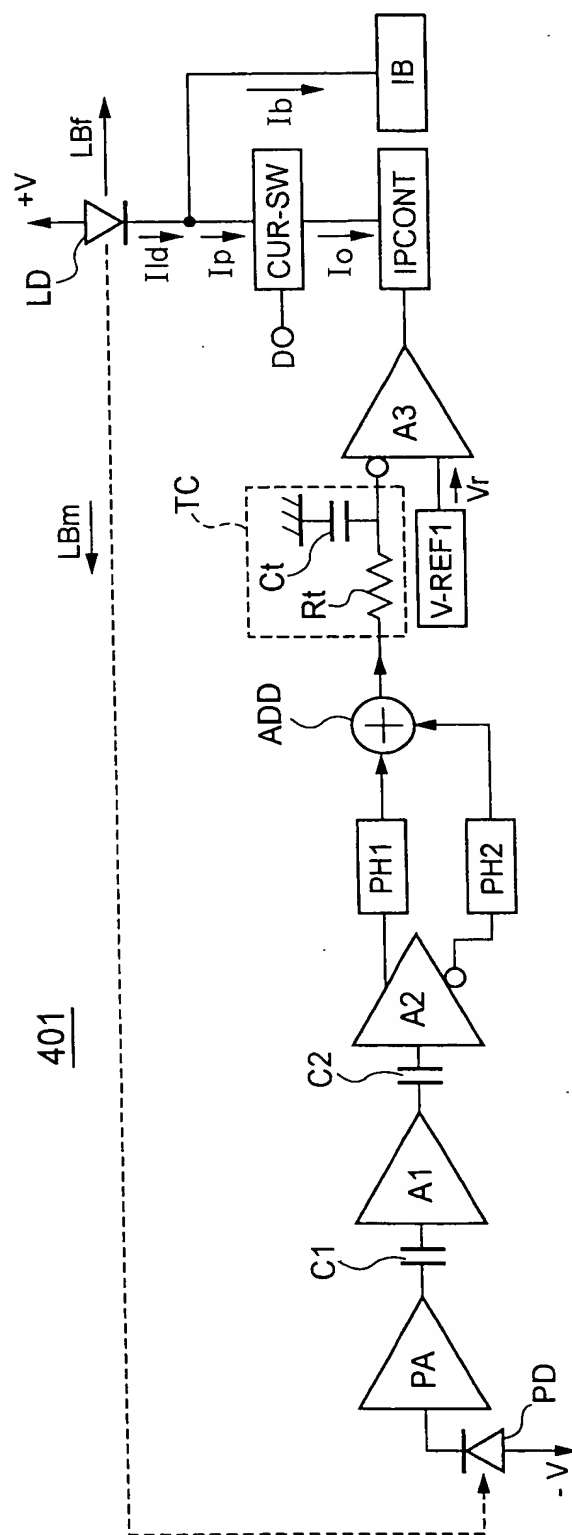


FIG. 15

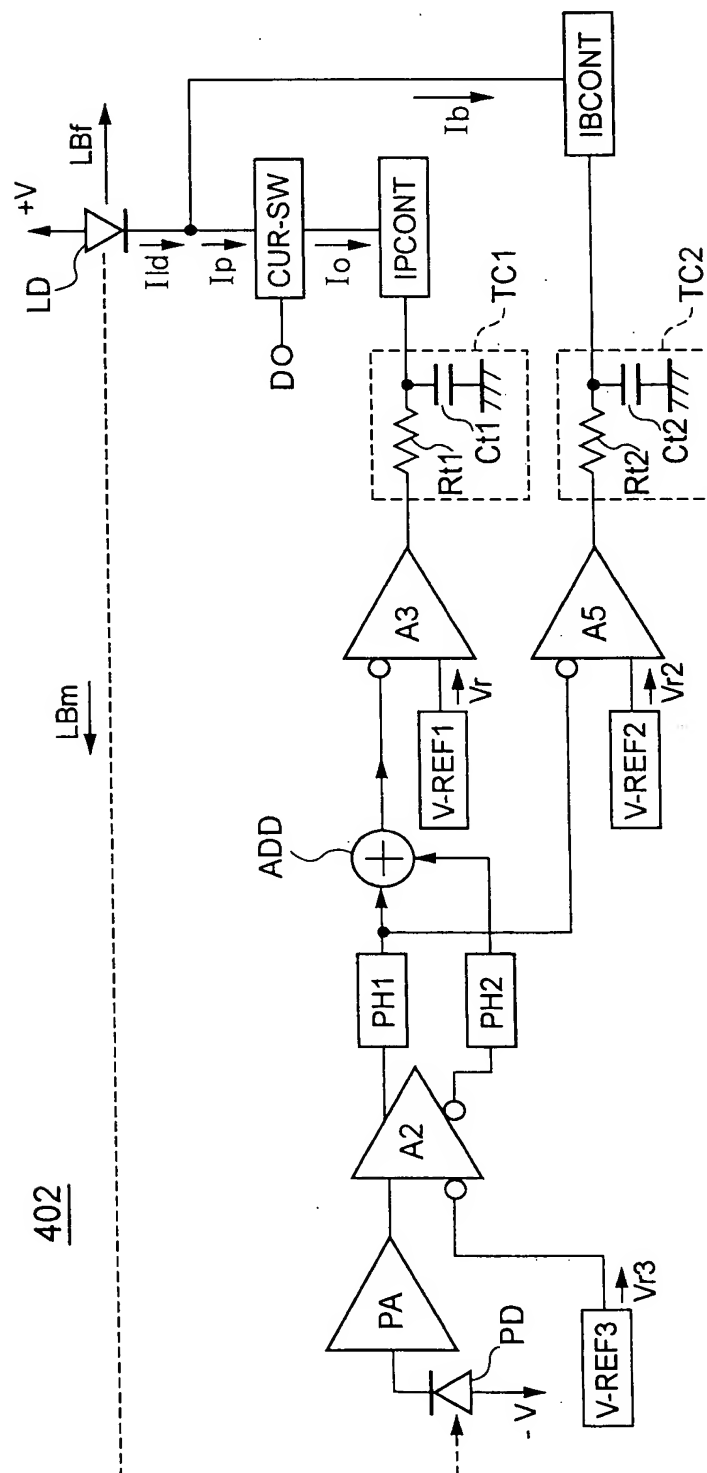


FIG. 16

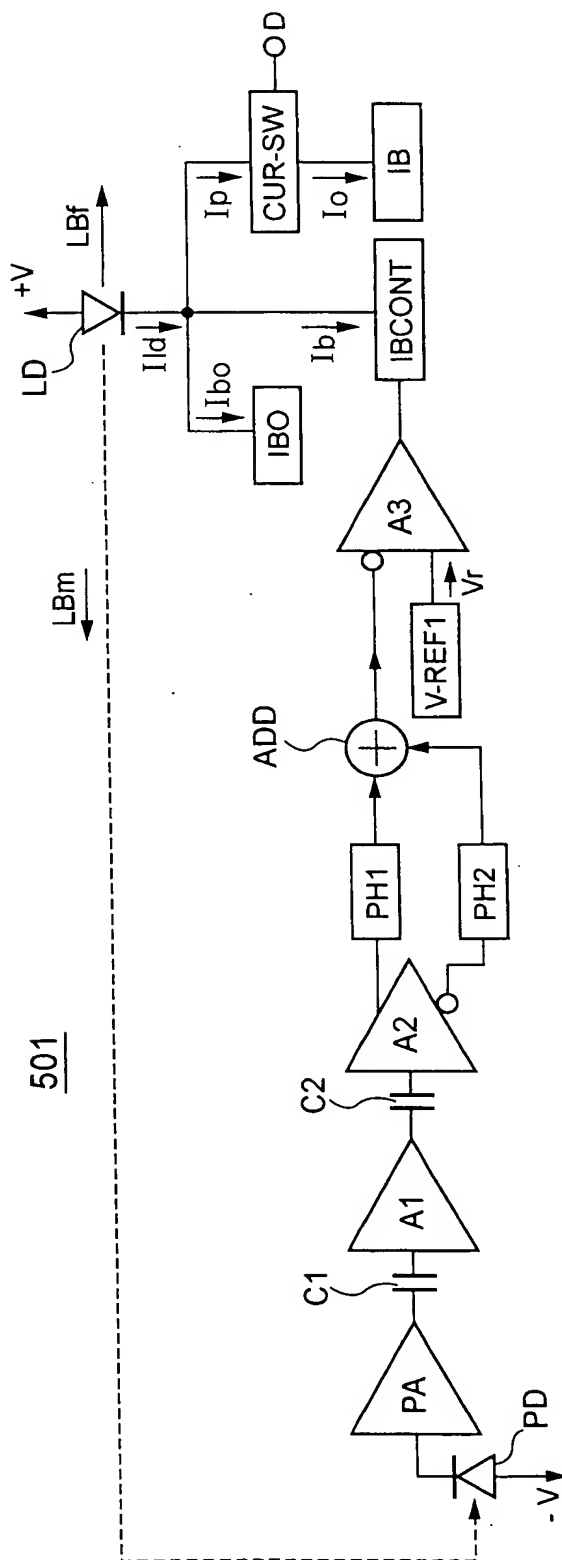


FIG. 18

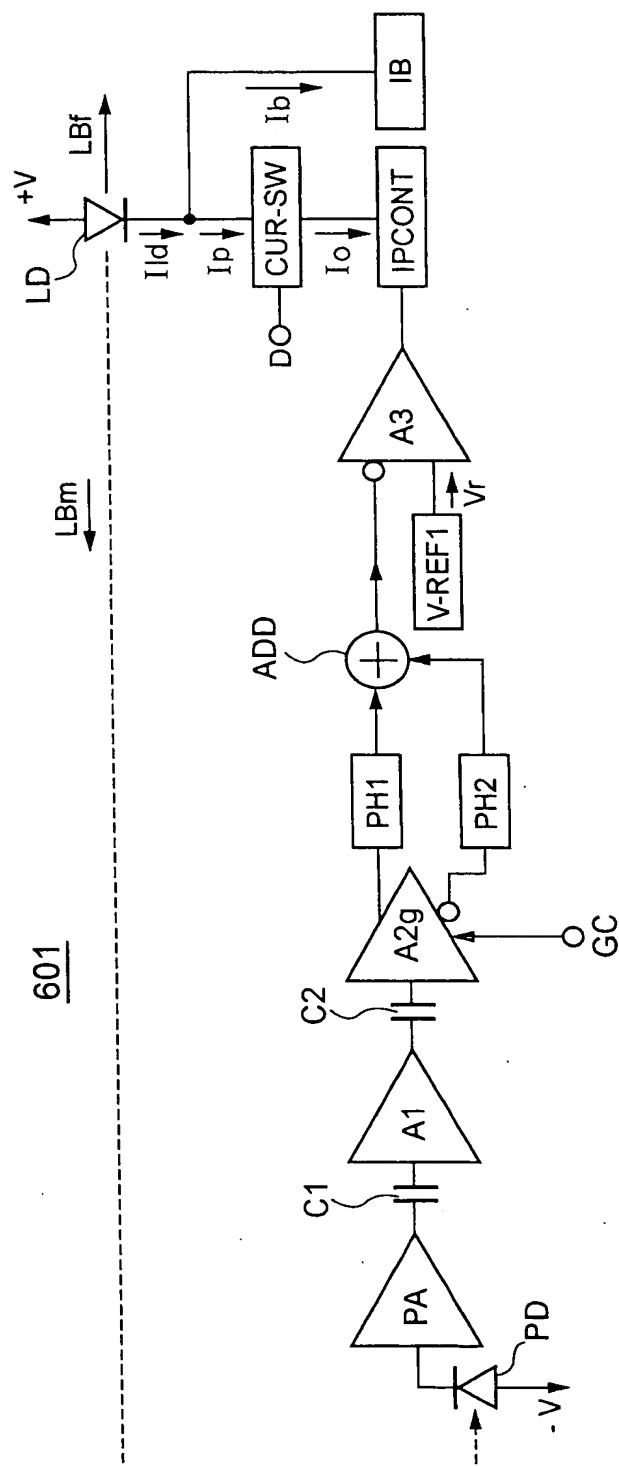


FIG. 19

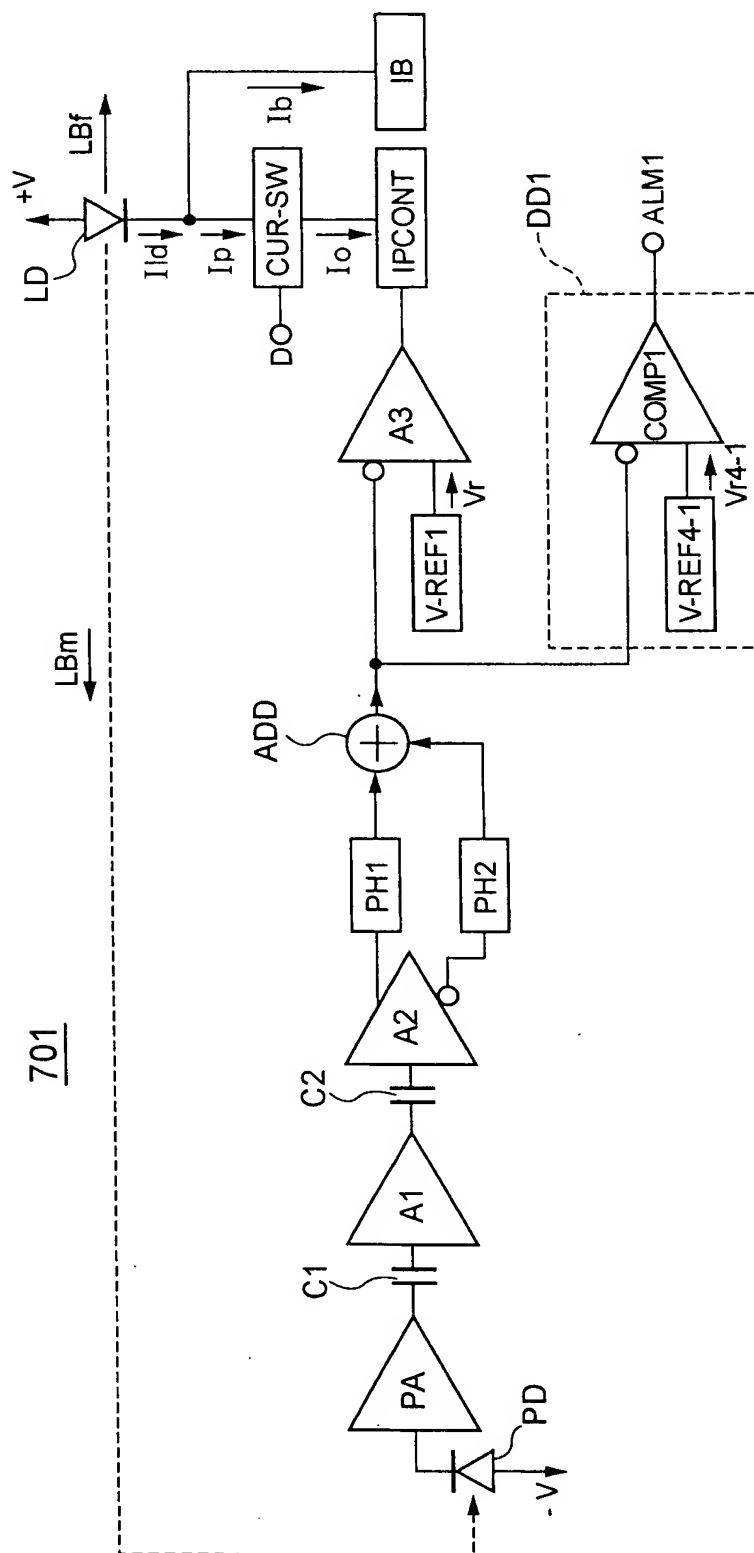


FIG. 20

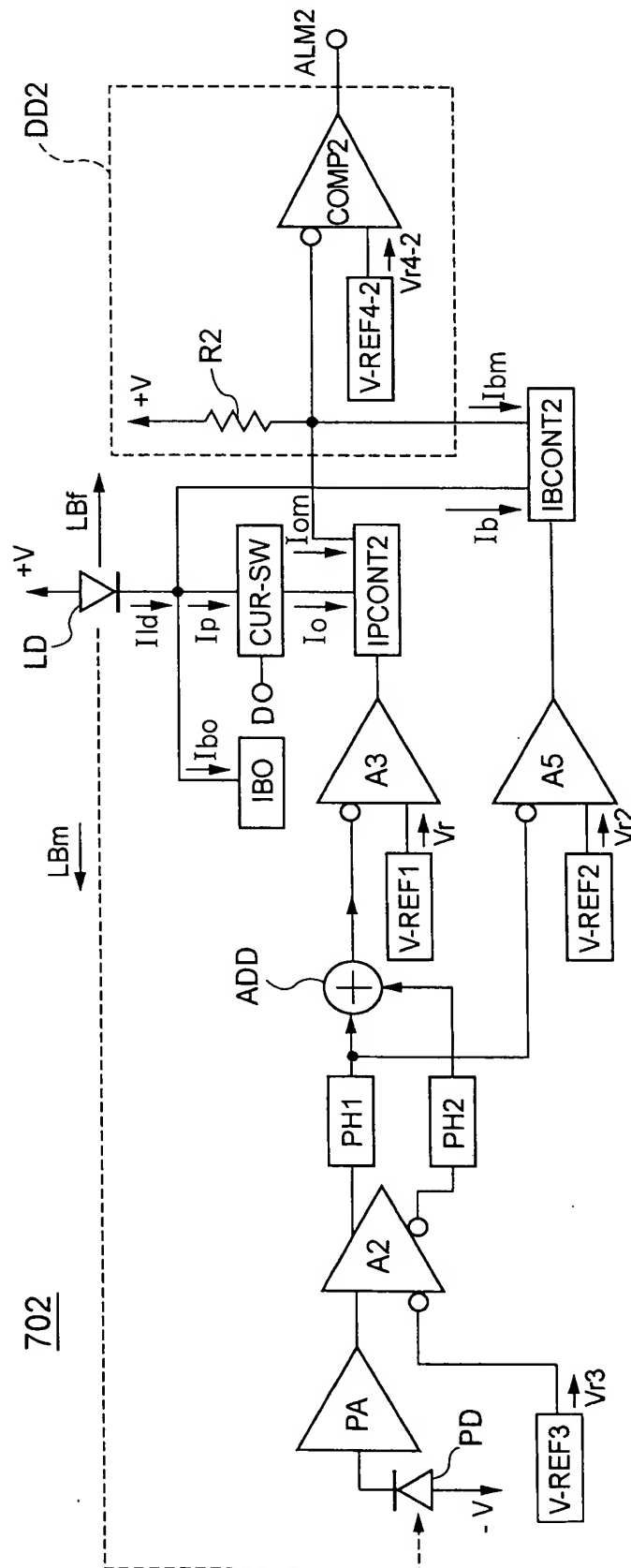
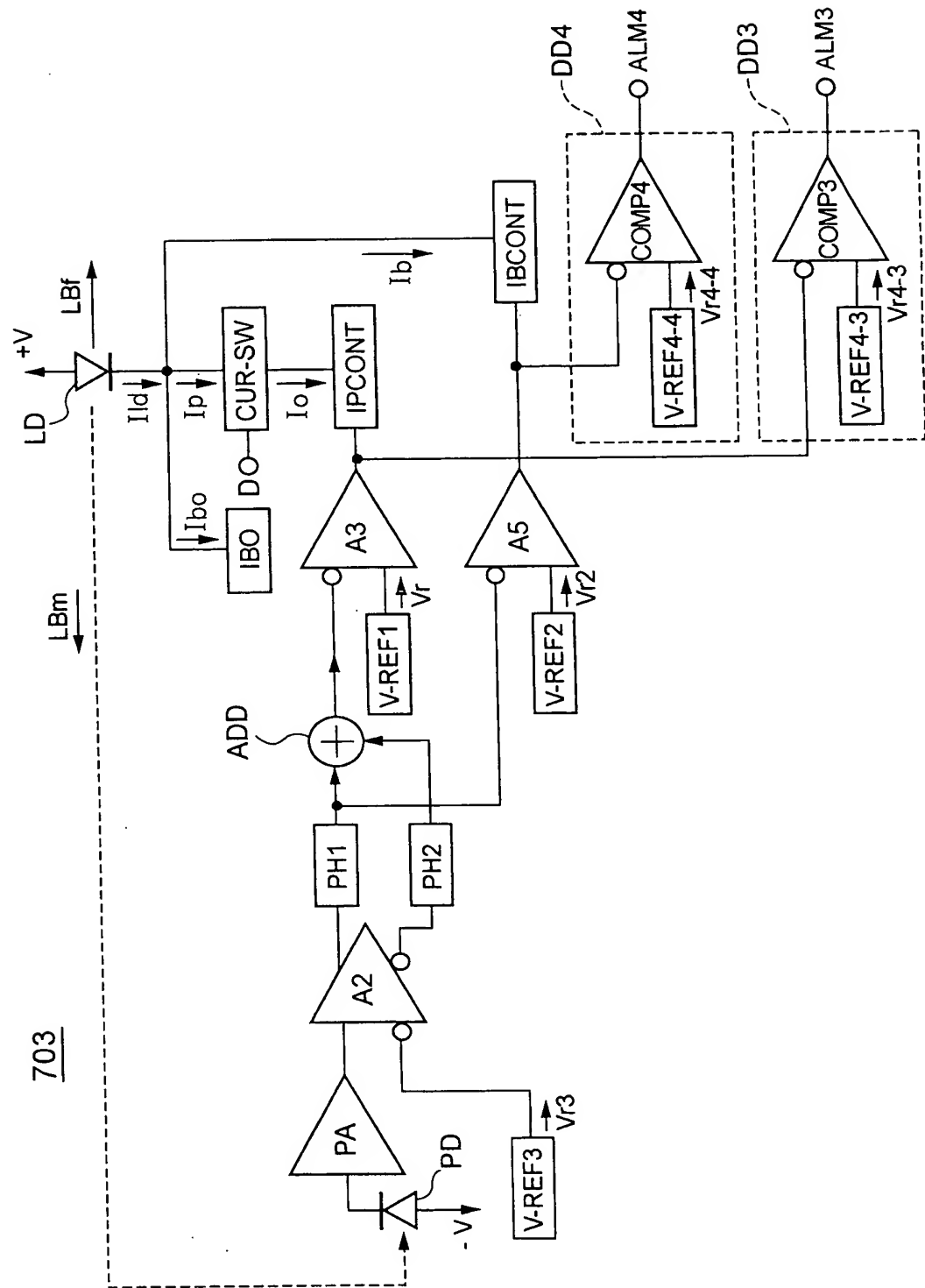
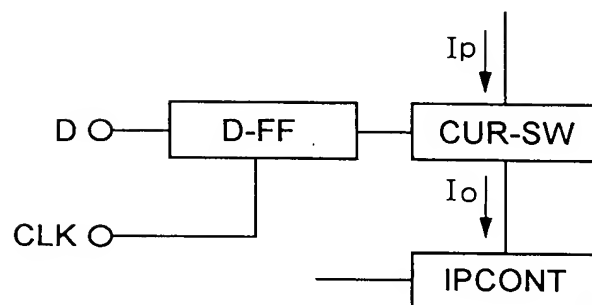


FIG. 21



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FIG. 22



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FIG. 23A

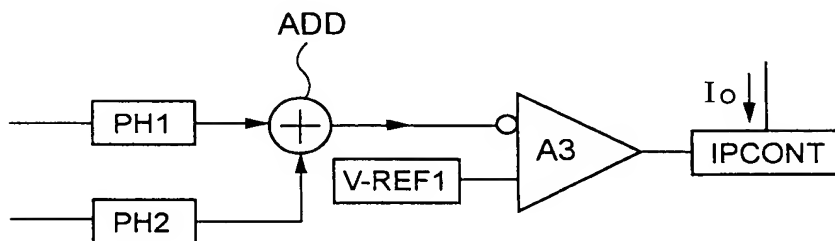


FIG. 23B

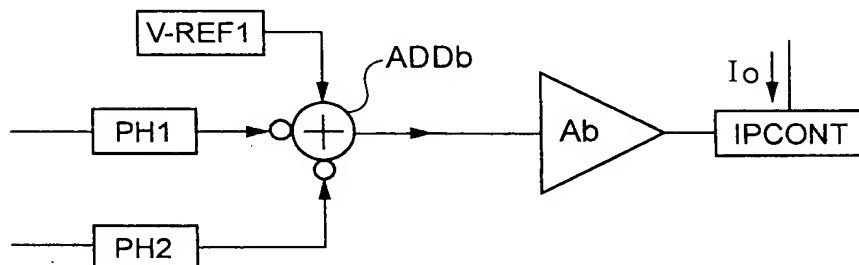


FIG. 23C

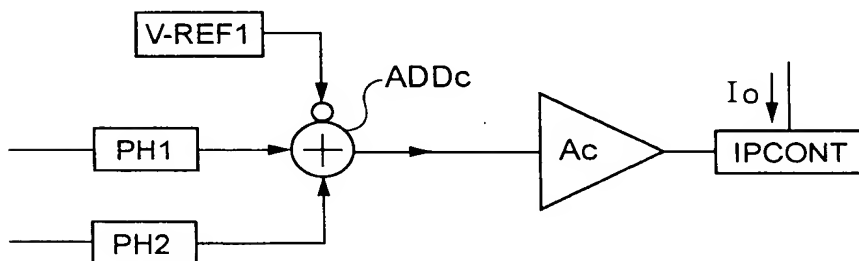
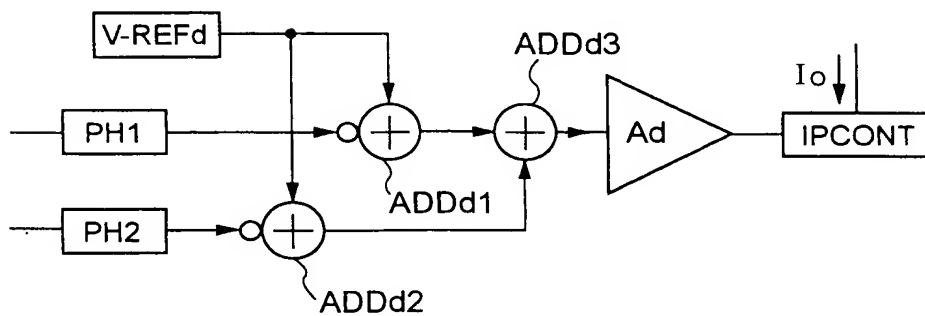


FIG. 23D



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FIG. 24A

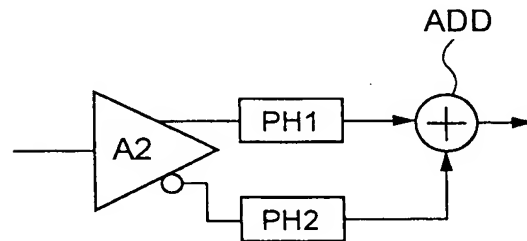


FIG. 24B

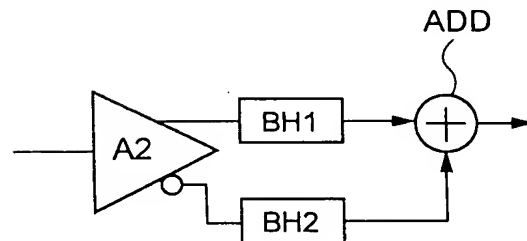


FIG. 24C

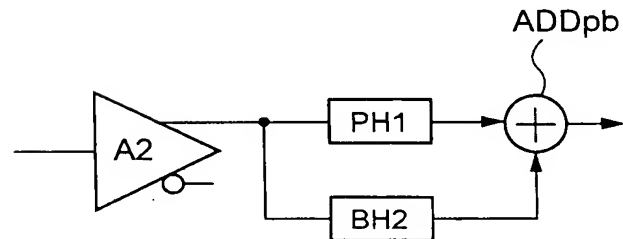


FIG. 25

